

EARTH ORBITER -1  
Level II Configuration Control Board  
CCR Distribution

EO-1 CCB Chairman: Pete Spidaliere

**EO-1 CCR No.:** 0007

**CCR TITLE:** Baseline Draft Issue of EO-1 WARP-LEISA ICD-057

**Date Issued:** January 21, 1998

**Due Date:** February 13, 1998

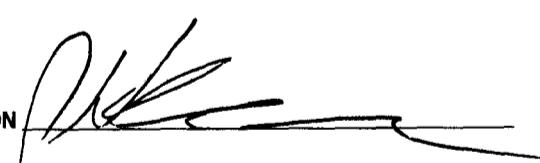
**CR Status:** Routine

Distribution List:

Terry Smith/GSFC	J. Bretthauer/GSFC
M.Perry/SWALES	E. Webb/GSFC
G.Jackson/GSFC	W. Powell/GSFC
J.Pocius/GSFC	J. Ramirez/GSFC
R.Whitley/GSFC	D. Molock/GSFC
S.Slegel/GSFC	B. Savage/GSFC
B.Parkinson/GSFC	M. Foreman/GSFC
J.Loiacono/GSFC	M.Kelley/GSFC
M.Jurotich/GSFC	B.Smith/GSFC
P.Spidalieri/GSFC	N.Speciale/GSFC
Vigg@ll/MIT	Digenis@ll/MIT
Bicknell@ll/MIT	Hoffeld@ll/MIT
CNICHOLS@CCGATE	BWKOPRA@CCGATE
PTBRYANT@CCGATE	U3DCR@LEPVAX.GSFC.NASA.GOV (Dennis Reuter)

EO-1 Configuration Manager: Steve Schneider/CSC/GSFC  
sschneider@hst.nasa.gov

## NEW MILLENNIUM PROJECT CONFIGURATION CHANGE REQUEST

PROGRAM <u>EO-1</u>	TITLE BASELINE EO-1 WARP AND LEISA/AC ICD-057							
CCR NO. <u>O R 0007 IN</u>	T O R _____ GSFC Code 735							
DATE INITIATED <u>O R 01/21/98 TO</u>	R'S C H G . N O . <u>EO-1 ICD-057</u>							
DUE DATE _____	SPONSOR/FUCODE <u>Dennis Reuter/Code 735</u> PHONE <u>x2042</u>							
EFFECTIVITY	CHANGE CLASS		TYPE OF CHANGE					
ITEM : <u>WARP/LEISA</u>	I	II	MILESTONE	<input type="checkbox"/>	INTERFACE	<input type="checkbox"/>	SOFTWARE	<input type="checkbox"/>
S/N _____	PRELIMINARY		DOCUMENT	<input type="checkbox"/>	POWER	<input type="checkbox"/>	OTHER	<input type="checkbox"/>
ITEM: _____	FORMAL		COST	<input type="checkbox"/>	WEIGHT	<input type="checkbox"/>	<u> </u>	
S/N _____	DOCUMENTS OR SOFTWARE AFFECTED <u>EO-1 ICD-057</u>							
ITEM: _____								
S / N								
PROBLEM								
<p>The attached draft version of EO1-ICD-057, Wide Band Advanced Recorder Processor (WARP) and Linear Etalon Imaging Spectral Arrar/Atmospheric Corrector (LEISA/AC) Interface Control Document (ICD) requires baselining. The document defines the functional, physical and electrical characteristics of the WARP and LEISA that impacts the EO-1 spacecraft.</p>								
PROPOSED SOLUTION								
<p>Approve the attached draft version of EO-1 ICD-057,WARP and LEISA/AC ICD by the EO-1 Level II Configuration Control Board (CCB). This draft issue will be formally released after CCB approval. Future changes will be initiated by submittal of Configuration Change Requests (CCRs) and Preliminary Interface Revision Notices (PIRNs) for CCB approval. This document is maintained by the EO-1 Configuration Management Office (CMO).</p>								
BOARD ACTION APPROVAL LEVEL CRITICALITY LEVEL PROCUREMENT CHANGE ORDER CLASSIFICATION								
APPROVE <input type="checkbox"/>	REQUIRED LEVEL I HQS	<input type="checkbox"/>	EMERGENCY <input type="checkbox"/>	ROUTINE	URGENT	EMERGENCY	<input type="checkbox"/>	
APPROVE WITH CHANGE E 4	LEVEL II GSFC	<input type="checkbox"/>	URGENT <input type="checkbox"/>	OPTION 1 <input type="checkbox"/>	OPTION 1 <input type="checkbox"/>			
DISAPPROVE <input type="checkbox"/>	LEVEL III	<input type="checkbox"/>	ROUTINE <input type="checkbox"/>	OPTION2 <input type="checkbox"/>	OPTION 2 <input type="checkbox"/>			
WITHDRAW <input type="checkbox"/>								
COMMENTS	<p>Approve w/ change to B/L ICD-057 WARP/LEISA ICD.</p> 							
CHAIRPERSON	DATE <u>11 MAR 98</u>							

EO-1 ICD-57  
Draft Issue  
January 21, 1998

**EO-1  
WIDEBAND ADVANCED RECORDER  
PROCESSOR  
(WARP)  
TO  
ATMOSPHERIC CORRECTOR  
(AC)  
INTERFACE CONTROL DOCUMENT  
(ICD)**

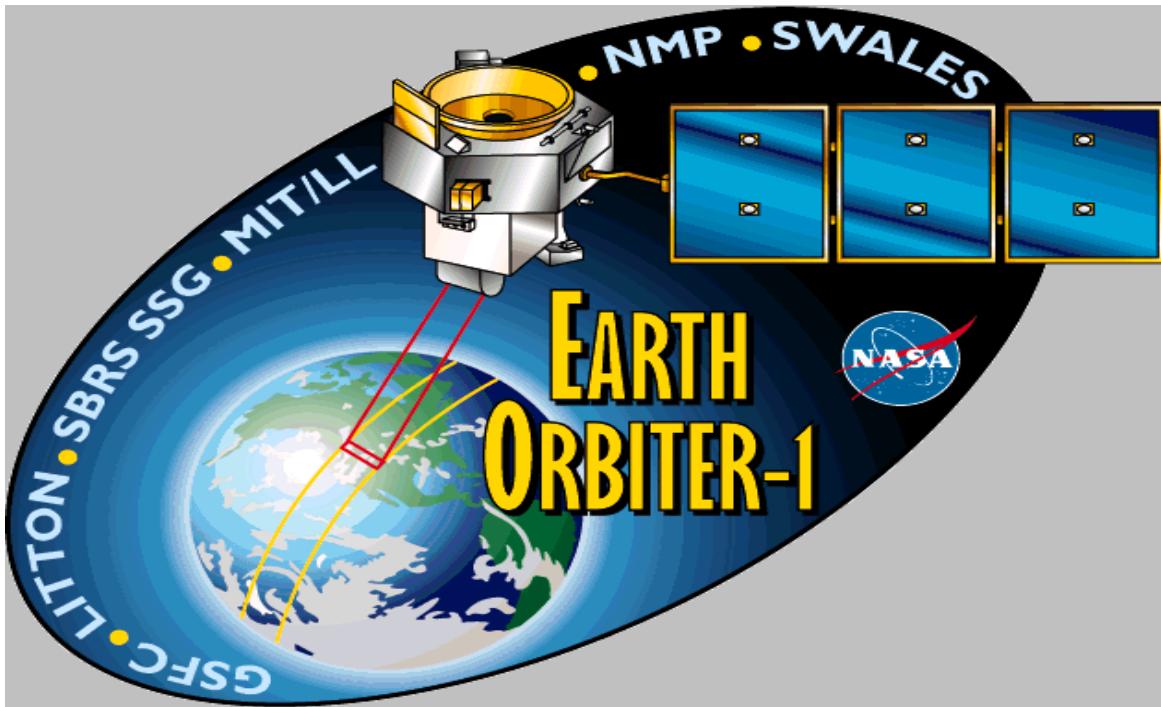


National Aeronautics and  
Space Administration

Goddard Space Flight Center  
Greenbelt, Maryland



NATIONAL AERONAUTICS AND SPACE ADMINISTRATION  
GODDARD SPACE FLIGHT CENTER



## EO-1 WARP Flight Hardware

---

# Atmospheric Corrector to Wideband Advanced Recorder Processor Interface Control Document

Version: Review

January 20, 1998



---

## REVISION HISTORY

**Preliminary Version**

6/11/97

**Rev. 1**

6/18/97

**Rev 2**

1/20/98

**Rev 3**

4/30/98

- Initial creation.
- Modified sections 2.5.3, 3.2.4. Added section 3.2.4.1
- Electrical specification
- TBS – Data format specification/to support WARP-AC testing



---

## TABLE OF CONTENTS

<b>1 OVERVIEW.....</b>	<b>1</b>
1.1 SCOPE.....	1
1.2 SUPPORTING DOCUMENTS.....	1
1.3 REQUIREMENTS.....	1
1.4 INTERFACE DESCRIPTION.....	1
1.4.1 WARP to AC Interface Description .....	1
1.5 INTERFACE LAYERS DESCRIPTION .....	1
<b>2 PHYSICAL LAYER.....</b>	<b>2</b>
2.1 PHYSICAL LAYER FUNCTION.....	2
2.2 MECHANICAL INTERFACE .....	2
2.2.1 Envelope.....	2
2.2.2 Coordinate System.....	2
2.2.3 Fasteners and Clamping .....	2
2.2.4 Alignment/Guide Grooves/Keying.....	Error! Bookmark not defined.
2.3 CABLE TYPE .....	3
2.3.1 Maximum Cable Length .....	3
2.3.2 Wire Gauge .....	3
2.3.3 Shield Connections .....	3
2.4 CONNECTOR TYPE.....	3
2.4.1 Connector Pin-Out.....	3
2.5 BIT LEVEL TIMING .....	4
2.5.1 Rise Time .....	4
2.5.2 Fall Time.....	4
2.5.3 Clock Frequency.....	4
2.6 SIGNAL LEVELS.....	5
2.6.1 Transmit Levels.....	5
2.6.2 Receive Levels.....	5
2.7 SIGNAL GROUNDING AND ISOLATION .....	5
2.8 HANDLING PROCEDURES.....	5
2.8.1 ESD Precautions.....	5
2.8.2 Connector Installation and Removal .....	5
2.8.3 Maximum Number of Mate-Demates .....	5
2.9 EMI/EMC/RFI SPECIFICATIONS AND PROCEDURES .....	5
<b>3 DATA LINK LAYER .....</b>	<b>5</b>
3.1 DATA LINK LAYER FUNCTION.....	6
3.2 DATA UNIT (FRAME) DEFINITION.....	6
3.2.1 Frame Data Area Size.....	6
3.2.2 Frame Header Definition .....	6
3.2.3 Frame Trailer Definition.....	7
3.3 DATA UNIT TIMING .....	8
3.3.1 Inter-Frame Gaps.....	8
<b>4 APPLICATION LAYER .....</b>	<b>8</b>

## 1 OVERVIEW

### 1.1 Scope

This document is the Interface Control Document between the Wide Band Advanced Recorder Processor (WARP) and Linear Etalon Imaging Spectral Array / Atmospheric Corrector (LEISA/AC or AC)

### 1.2 Supporting Documents

Spec ID	Title	Source	Date
	<u>Computer Networks</u> , 2 ed., by Andrew Tanenbaum	in GSFC library	1989
	<u>OSI Explained</u> , by John Henshall and Sandy Shaw	in GSFC library	1988
AM-149-0020(155)	<u>System Level Electrical Requirements</u> <u>NMP EO-1 Flight</u>	Litton Amecon	1996
	<u>FUSE Science Data Bus ICD</u> , by Terry Smith	Terry Smith or Evan Webb	1993

### 1.3 Requirements

The WARP / AC interface is made up of mechanical and electrical constituents. The mechanical interface consists of a 78-pin connector and associated wiring harness. The electrical interface consists of a 32-bit differential data bus and two differential control signals.

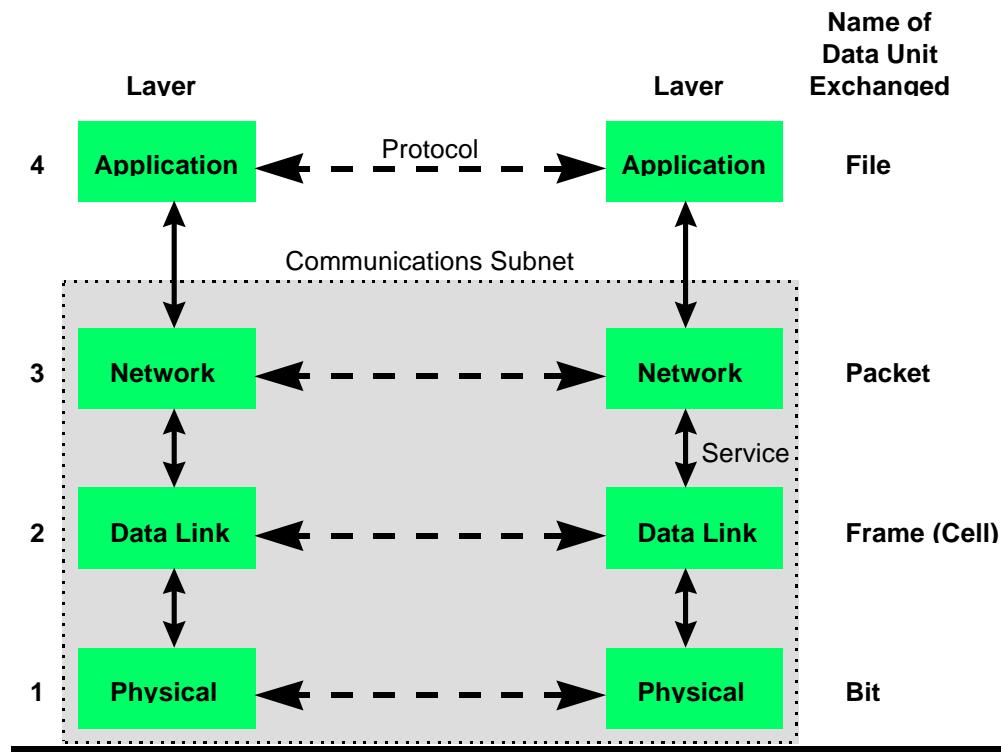
### 1.4 Interface Description

#### 1.4.1 WARP to AC Interface Description

The interface to the WARP is via an intermediate assembly that converts RS-422 electrical levels to Fiber Optic signals. The specifics of the interface are described in the following sections.

### 1.5 Interface Layers Description

This document will use a modified Open Systems Interconnect (OSI) standard model which describes an interface between two systems. Each system performs functions which can be described as a series of layers. Each system has the same number and function of layers, and the equivalent layers for each system communicate via an established protocol which is transparent to the protocols at other layers. Each system passes data from its upper layers to the lower layers via a service provided by the next lower layer. OSI uses seven layers to describe an interface, for the purpose of this document we will use four layers; the Physical Layer (Layer 1), the Data Link Layer (Layer 2), the Network Layer (Layer 3), and the Application Layer (Layer 4). The first three layers are identical to those of the OSI standard, and comprise what is known as the communication subnet. The fourth layer corresponds to the upper software-oriented functions of the interface in the OSI standard (Transport Layer, Session Layer, Presentation Layer, and Application Layer.) Figure 2 illustrates the layer concept.



## 2 PHYSICAL LAYER

### 2.1 Physical Layer Function

The Physical Layer consists of two parts: the physical layer medium (the cabling and connectors, etc. that make up the physical connection between the two systems) and the physical layer protocol that defines the lowest level of formatting (bit-level) of the data. The Physical Layer description should be limited to only those parts of the interface.

### 2.2 Mechanical Interface

#### 2.2.1 Envelope

The mechanical envelope of the WARP to AC interface is defined by an imaginary box that would encase a 78-pin Subminiature D connector and its associated mating hardware.

#### 2.2.2 Coordinate System

We will use Figure 3.2.1-2 from the EO-1 to LAC ICD to define the AC coordinates.

#### 2.2.3 Fasteners and Clamping

The fasteners and clamping for the AC / WARP shall be standard mating hardware for a 78-pin Subminiature D connector.

#### 2.2.4 Thermal Interface

There is no thermal requirement between the WARP and AC.

## 2.3 Cable Type

### 2.3.1 Maximum Cable Length

The interface to the WARP is through an intermediate assembly that converts the RS-422 differential signals to fiber optic signals. The maximum cable length is 12 feet.

### 2.3.2 Wire Gauge

The wires of the WARP / AC harness are 22-gauge.

### 2.3.3 Shield Connections

The shield connections of the AC / WARP harness shall conform to Doc. No. AM149-0020(155).

## 2.4 Connector Type

The WARP-AC interface consists of a 78-pin D Subminiature (DB-78) plug-type connector (Part Number M24308/8-349).

### 2.4.1 Connector Pin-Out

#### Connector ( DB 78 ) Pin Out

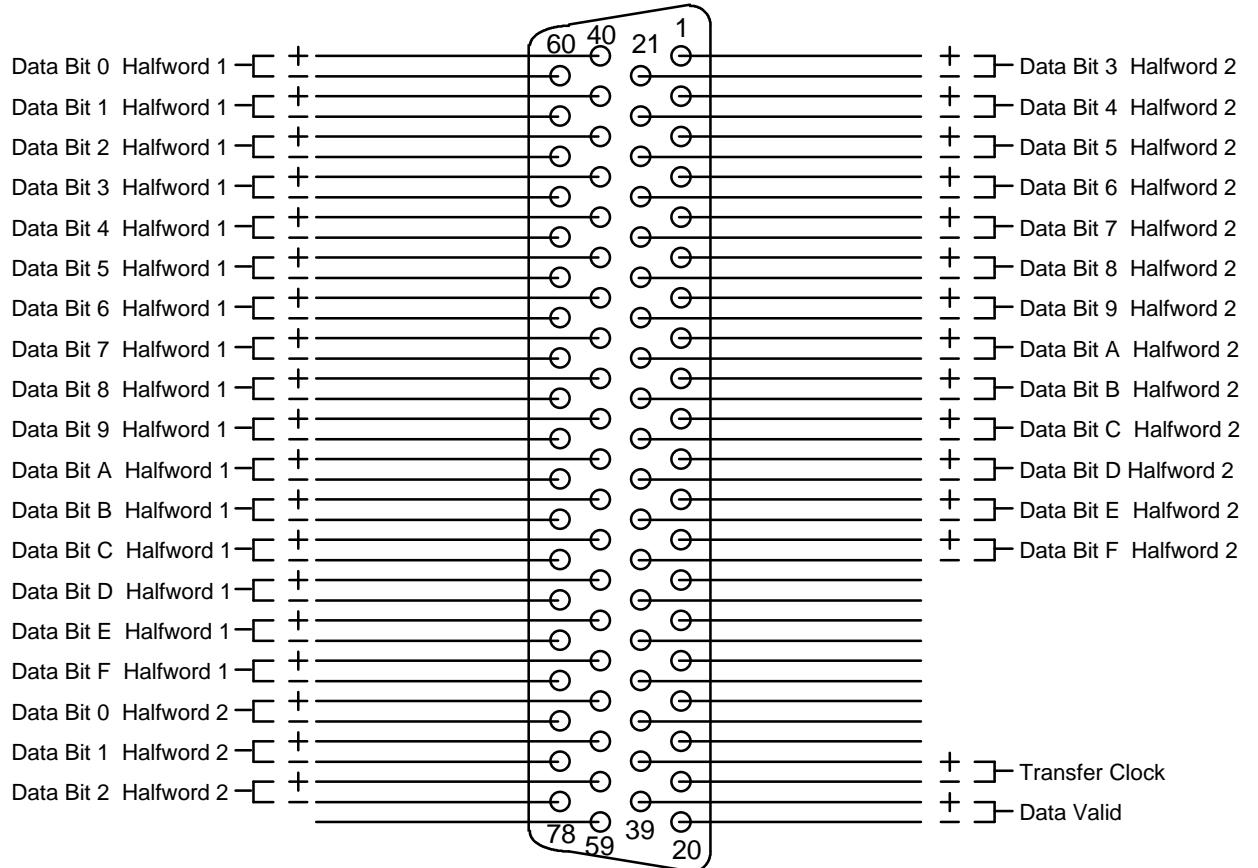


FIGURE 2.4.1

### 2.4.2 AC to WARP Signal Mapping

<u>Instrument Pin Name</u>	<u>WARP Pin Name</u>	<u>Pin Number</u>
Data Bit F Halfword2_P	AC_DB31P	13
Data Bit F Halfword2_N	AC_DB31N	33
Data Bit E Halfword2_P	AC_DB30P	12
Data Bit E Halfword2_N	AC_DB30N	32
Data Bit D Halfword2_P	AC_DB29P	11
Data Bit D Halfword2_N	AC_DB29N	31
Data Bit C Halfword2_P	AC_DB28P	10
Data Bit C Halfword2_N	AC_DB28N	30
Data Bit B Halfword2_P	AC_DB27P	9
Data Bit B Halfword2_N	AC_DB27N	29
Data Bit A Halfword2_P	AC_DB26P	8
Data Bit A Halfword2_N	AC_DB26N	28
Data Bit 9 Halfword2_P	AC_DB25P	7
Data Bit 9 Halfword2_N	AC_DB25N	27
Data Bit 8 Halfword2_P	AC_DB24P	6
Data Bit 8 Halfword2_N	AC_DB24N	26
Data Bit 7 Halfword2_P	AC_DB23P	5
Data Bit 7 Halfword2_N	AC_DB23N	25
Data Bit 6 Halfword2_P	AC_DB22P	4
Data Bit 6 Halfword2_N	AC_DB22N	24
Data Bit 5 Halfword2_P	AC_DB21P	3
Data Bit 5 Halfword2_N	AC_DB21N	23
Data Bit 4 Halfword2_P	AC_DB20P	2
Data Bit 4 Halfword2_N	AC_DB20N	22
Data Bit 3 Halfword2_P	AC_DB19P	1
Data Bit 3 Halfword2_N	AC_DB19N	21
Data Bit 2 Halfword2_P	AC_DB18P	58
Data Bit 2 Halfword2_N	AC_DB18N	78
Data Bit 1 Halfword2_P	AC_DB17P	57
Data Bit 1 Halfword2_N	AC_DB17N	77
Data Bit 0 Halfword2_P	AC_DB16P	56
Data Bit 0 Halfword2_N	AC_DB16N	76
Data Bit F Halfword1_P	AC_DB15P	55
Data Bit F Halfword1_N	AC_DB15N	75
Data Bit E Halfword1_P	AC_DB14P	54
Data Bit E Halfword1_N	AC_DB14N	74
Data Bit D Halfword1_P	AC_DB13P	53
Data Bit D Halfword1_N	AC_DB13N	73
Data Bit C Halfword1_P	AC_DB12P	52
Data Bit C Halfword1_N	AC_DB12N	72
Data Bit B Halfword1_P	AC_DB11P	51
Data Bit B Halfword1_N	AC_DB11N	71
Data Bit A Halfword1_P	AC_DB10P	50

Data Bit A Halfword1_N	AC_DB10N	70
Data Bit 9 Halfword1_P	AC_DB9P	49
Data Bit 9 Halfword1_N	AC_DB9N	69
Data Bit 8 Halfword1_P	AC_DB8P	48
Data Bit 8 Halfword1_N	AC_DB8N	68
Data Bit 7 Halfword1_P	AC_DB7P	47
Data Bit 7 Halfword1_N	AC_DB7N	67
Data Bit 6 Halfword1_P	AC_DB6P	46
Data Bit 6 Halfword1_N	AC_DB6N	66
Data Bit 5 Halfword1_P	AC_DB5P	45
Data Bit 5 Halfword1_N	AC_DB5N	65
Data Bit 4 Halfword1_P	AC_DB4P	44
Data Bit 4 Halfword1_N	AC_DB4N	64
Data Bit 3 Halfword1_P	AC_DB3P	43
Data Bit 3 Halfword1_N	AC_DB3N	63
Data Bit 2 Halfword1_P	AC_DB2P	42
Data Bit 2 Halfword1_N	AC_DB2N	62
Data Bit 1 Halfword1_P	AC_DB1P	41
Data Bit 1 Halfword1_N	AC_DB1N	61
Data Bit 0 Halfword1_P	AC_DB0P	40
Data Bit 0 Halfword1_N	AC_DB0N	60
Transfer Clock_P	AC_CLKP	38
Transfer Clock_N	AC_CLKN	19
Data Valid_P	AC_VALIDP	39
Data Valid_N	AC_VALIDN	20

## 2.5 Bit Level Timing

### 2.5.1 Rise Time

The rise time of the AC data lines is 1 nSecond min. and TBD nSecond max.

### 2.5.2 Fall Time

The fall time of the AC data lines is 1 nSecond min. and TBD nSecond max.

### 2.5.3 Clock Frequency

The data clock has two speeds 6.0 MHz and 3.0 MHz. The data clock is only set to the 6.0 MHz rate during periods that the ALI is not on and the AC is set for a 60 Hz frame rate. The data clock is set for 3.0 MHz for all other frame rates. For the slower frame rates, e.g. 2 Hz, 7.5 Hz, and 15 Hz, the data buffers may empty giving intra-frame gaps in the data coming over the RS-422 link. During these gaps, the data ready bit will remain low.

### 2.5.4 Timing Diagrams

Figures 2.5.4.1 and 2.5.4.2 show the bit level timing for data transfers with respect to the data transfer clock and the data ready signals.

FIGURE 2.5.4.1

FIGURE 2.5.4.2

## 2.6 Signal Levels

### 2.6.1 Transmit Levels

The low level output voltage of transmitted signals is 0.5V maximum. The high level output voltage of transmitted signals is 2.5V minimum.

### 2.6.2 Receive Levels

The low level output voltage of received signals is 0.3V maximum. The high level output voltage of received signals it 3.8V minimum.

## 2.7 Signal Grounding and Isolation

The signal grounding and isolation of the AC / WARP interface shall conform to Doc. No. AM149-0020(155).

## 2.8 Handling Procedures

### 2.8.1 ESD Precautions

The AC instrument hardware will be handled using standard ESD safeguards for space flight equipment.

## 2.9 EMI/EMC/RFI Specifications and Procedures

AC to WARP RS-422 Interface will comply with EO-1 Verification Plan and Environmental Specification SAI-SPEC-158

# 3 DATA LINK LAYER

## 3.1 Data Link Layer Function

The Data Link Layer defines the basic data units, usually called frames, which are present on the interface and ensures that they are transmitted free of errors from the source to the destination. The frames are created by adding headers and /or trailers to the data at the source which are recognized by the Data Link Layer service in the receiver. These frames can serve as sync patterns and also as the extra bits required for frame error detection and correction. The other principal function of this layer is flow control: managing the volume of data from source to destination so as to prevent overflow or underflow of the buffers on either end. Both flow control and error control require acknowledgment from receiver to source, and this acknowledgment scheme is defined at this layer.

## 3.2 Data Unit (Frame) Definition

### 3.2.1 Frame Data Area Size

A frame for the AC consists of a frame header of 512 half-words and three 256 X 256 pixel array samples of 1 half-word each (for a total of 3.153920 Mbits).

### 3.2.2 Frame Header Definition

The frame header is defined in Figure 3.3.2. It consists of 2 half-words all set to logic level 1 signifying a beginning of frame. The frame start is followed by mission timing data acquired from the spacecraft master clock for time stamping of the data collected. There is a frame counter for counting the frames during a certain 1 second interval. Finally, the temperature of each array as read from the on-chip temperature sensors is recorded. At the end of the frame header there are 500 half-words that are currently spares.

## LEISA/AC Data Header Format

Header: 512 Halfwords ( 16 bits/Halfword )

0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F

Frame Start - 32 Bits All Set To "1"  
 Two Halfwords

0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---

Days: Range 0-366  
 One Halfword

0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---

Hours: Range 0-23  
 One Halfword

0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---

Minutes: Range 0-59  
 One Halfword

0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---

Seconds: Range 0-59  
 One Halfword

0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F

Microseconds: Range 0-999,000

Microseconds: 4 MS Bits

Microseconds: 16 LS Bits

0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---

Offset Counter ( 8 Bits )  
 One Halfword

0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---

Focal Plane 1 Temperature ( Voltage )  
 One Halfword

0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---

Focal Plane 2 Temperature ( Voltage )  
 One Halfword

0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---

Focal Plane 3 Temperature ( Voltage )  
 One Halfword

0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---

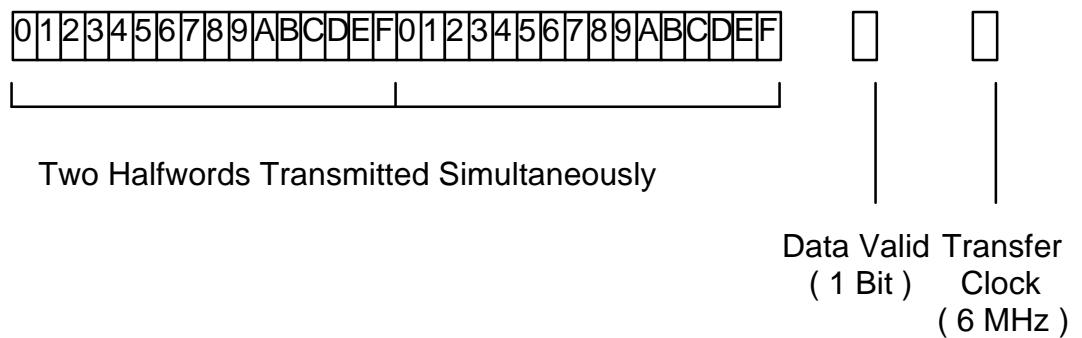
Spare: 500 Halfwords

### FIGURE 3.2.2

#### 3.2.3 Frame Trailer Definition

The LEISA/AC does not have a trailer.

#### 3.2.4 Frame Timing



### 3.3 Data Unit Timing

#### 3.3.1 Inter-Frame Gaps

The data header is constructed by the UT69R000 micro-controller at the time that the frame start command is received. The data header is transmitted across the science data bus to the WARP as soon as it is completed. Immediately following the data header, the science data is transmitted from dual port memory to the data bus. There may be inter-frame gaps in the data transmission of up to 320 usec during those times the data valid signal will remain low.

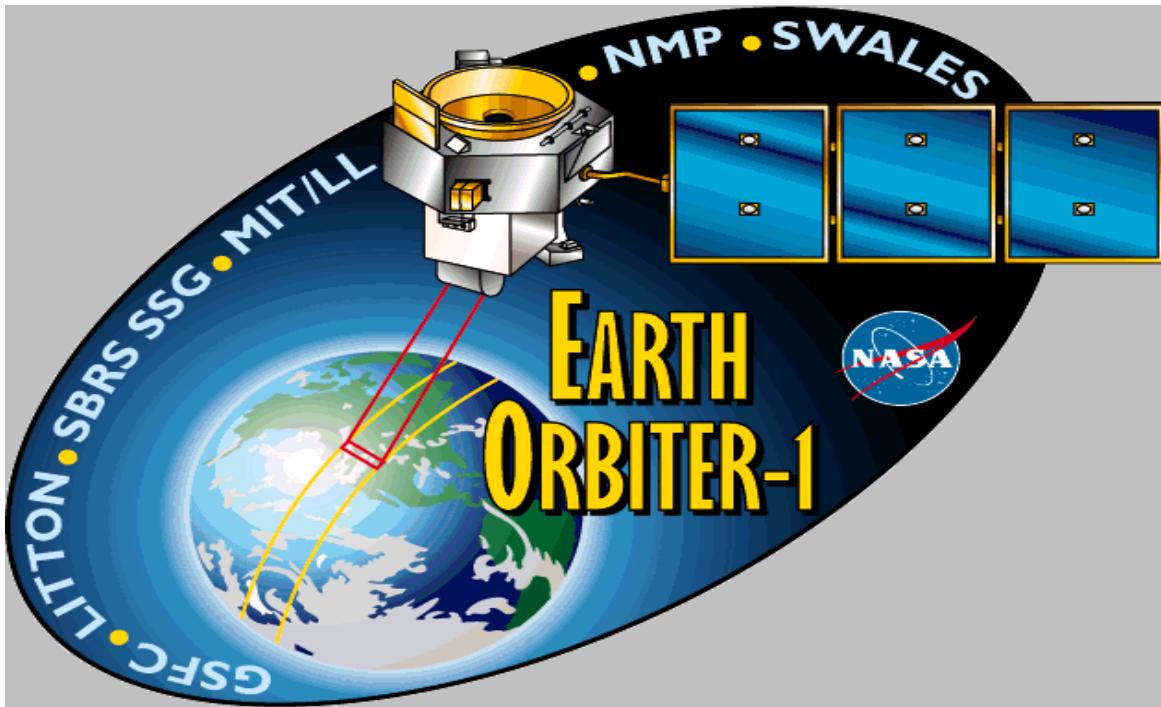
## 4 NETWORK LAYER AND APPLICATION LAYERS

TBD

**NOTE:** This section will be provided by the AC team by the April 30, 1998 timeframe and approved through a future CCR process. This section will contain sufficient information to validate data content, structure and volume from the AC interface through WARP IGSE.



NATIONAL AERONAUTICS AND SPACE ADMINISTRATION  
GODDARD SPACE FLIGHT CENTER



## EO-1 WARP Flight Hardware

---

# Atmospheric Corrector to Wideband Advanced Recorder Processor Interface Control Document

Version: Review

January 20, 1998



---

## REVISION HISTORY

**Preliminary Version**

6/11/97

**Rev. 1**

6/18/97

**Rev 2**

1/20/98

**Rev 3**

4/30/98

- Initial creation.
- Modified sections 2.5.3, 3.2.4. Added section 3.2.4.1
- Electrical specification
- TBS – Data format specification/to support WARP-AC testing



---

## TABLE OF CONTENTS

<b>1 OVERVIEW.....</b>	<b>1</b>
1.1 SCOPE.....	1
1.2 SUPPORTING DOCUMENTS.....	1
1.3 REQUIREMENTS.....	1
1.4 INTERFACE DESCRIPTION.....	1
1.4.1 WARP to AC Interface Description .....	1
1.5 INTERFACE LAYERS DESCRIPTION .....	1
<b>2 PHYSICAL LAYER.....</b>	<b>2</b>
2.1 PHYSICAL LAYER FUNCTION.....	2
2.2 MECHANICAL INTERFACE .....	2
2.2.1 Envelope.....	2
2.2.2 Coordinate System.....	2
2.2.3 Fasteners and Clamping .....	2
2.2.4 Alignment/Guide Grooves/Keying.....	Error! Bookmark not defined.
2.3 CABLE TYPE .....	3
2.3.1 Maximum Cable Length .....	3
2.3.2 Wire Gauge .....	3
2.3.3 Shield Connections .....	3
2.4 CONNECTOR TYPE.....	3
2.4.1 Connector Pin-Out.....	3
2.5 BIT LEVEL TIMING .....	4
2.5.1 Rise Time .....	4
2.5.2 Fall Time.....	4
2.5.3 Clock Frequency.....	4
2.6 SIGNAL LEVELS.....	5
2.6.1 Transmit Levels.....	5
2.6.2 Receive Levels.....	5
2.7 SIGNAL GROUNDING AND ISOLATION .....	5
2.8 HANDLING PROCEDURES.....	5
2.8.1 ESD Precautions.....	5
2.8.2 Connector Installation and Removal .....	5
2.8.3 Maximum Number of Mate-Demates .....	5
2.9 EMI/EMC/RFI SPECIFICATIONS AND PROCEDURES .....	5
<b>3 DATA LINK LAYER .....</b>	<b>5</b>
3.1 DATA LINK LAYER FUNCTION.....	6
3.2 DATA UNIT (FRAME) DEFINITION.....	6
3.2.1 Frame Data Area Size.....	6
3.2.2 Frame Header Definition .....	6
3.2.3 Frame Trailer Definition.....	7
3.3 DATA UNIT TIMING .....	8
3.3.1 Inter-Frame Gaps.....	8
<b>4 APPLICATION LAYER .....</b>	<b>8</b>

## 1 OVERVIEW

### 1.1 Scope

This document is the Interface Control Document between the Wide Band Advanced Recorder Processor (WARP) and Linear Etalon Imaging Spectral Array / Atmospheric Corrector (LEISA/AC or AC)

### 1.2 Supporting Documents

Spec ID	Title	Source	Date
	<u>Computer Networks</u> , 2 ed., by Andrew Tanenbaum	in GSFC library	1989
	<u>OSI Explained</u> , by John Henshall and Sandy Shaw	in GSFC library	1988
AM-149-0020(155)	<u>System Level Electrical Requirements</u> <u>NMP EO-1 Flight</u>	Litton Amecon	1996
	<u>FUSE Science Data Bus ICD</u> , by Terry Smith	Terry Smith or Evan Webb	1993

### 1.3 Requirements

The WARP / AC interface is made up of mechanical and electrical constituents. The mechanical interface consists of a 78-pin connector and associated wiring harness. The electrical interface consists of a 32-bit differential data bus and two differential control signals.

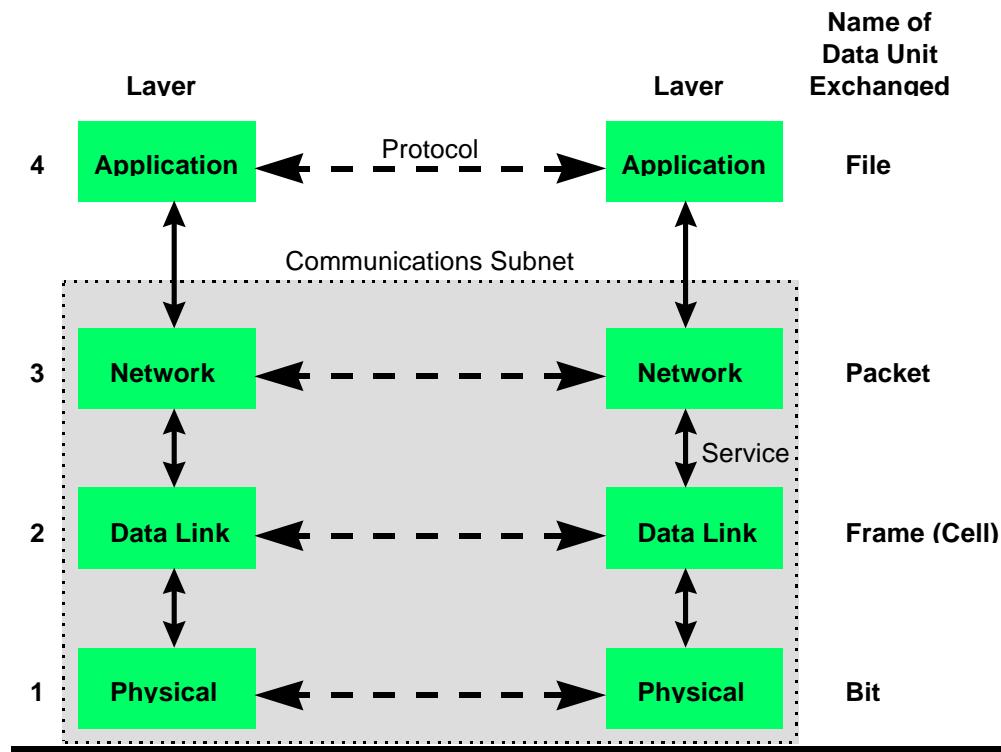
### 1.4 Interface Description

#### 1.4.1 WARP to AC Interface Description

The interface to the WARP is via an intermediate assembly that converts RS-422 electrical levels to Fiber Optic signals. The specifics of the interface are described in the following sections.

### 1.5 Interface Layers Description

This document will use a modified Open Systems Interconnect (OSI) standard model which describes an interface between two systems. Each system performs functions which can be described as a series of layers. Each system has the same number and function of layers, and the equivalent layers for each system communicate via an established protocol which is transparent to the protocols at other layers. Each system passes data from its upper layers to the lower layers via a service provided by the next lower layer. OSI uses seven layers to describe an interface, for the purpose of this document we will use four layers; the Physical Layer (Layer 1), the Data Link Layer (Layer 2), the Network Layer (Layer 3), and the Application Layer (Layer 4). The first three layers are identical to those of the OSI standard, and comprise what is known as the communication subnet. The fourth layer corresponds to the upper software-oriented functions of the interface in the OSI standard (Transport Layer, Session Layer, Presentation Layer, and Application Layer.) Figure 2 illustrates the layer concept.



## 2 PHYSICAL LAYER

### 2.1 Physical Layer Function

The Physical Layer consists of two parts: the physical layer medium (the cabling and connectors, etc. that make up the physical connection between the two systems) and the physical layer protocol that defines the lowest level of formatting (bit-level) of the data. The Physical Layer description should be limited to only those parts of the interface.

### 2.2 Mechanical Interface

#### 2.2.1 Envelope

The mechanical envelope of the WARP to AC interface is defined by an imaginary box that would encase a 78-pin Subminiature D connector and its associated mating hardware.

#### 2.2.2 Coordinate System

We will use Figure 3.2.1-2 from the EO-1 to LAC ICD to define the AC coordinates.

#### 2.2.3 Fasteners and Clamping

The fasteners and clamping for the AC / WARP shall be standard mating hardware for a 78-pin Subminiature D connector.

#### 2.2.4 Thermal Interface

There is no thermal requirement between the WARP and AC.

## 2.3 Cable Type

### 2.3.1 Maximum Cable Length

The interface to the WARP is through an intermediate assembly that converts the RS-422 differential signals to fiber optic signals. The maximum cable length is 12 feet.

### 2.3.2 Wire Gauge

The wires of the WARP / AC harness are 22-gauge.

### 2.3.3 Shield Connections

The shield connections of the AC / WARP harness shall conform to Doc. No. AM149-0020(155).

## 2.4 Connector Type

The WARP-AC interface consists of a 78-pin D Subminiature (DB-78) plug-type connector (Part Number M24308/8-349).

### 2.4.1 Connector Pin-Out

#### Connector ( DB 78 ) Pin Out

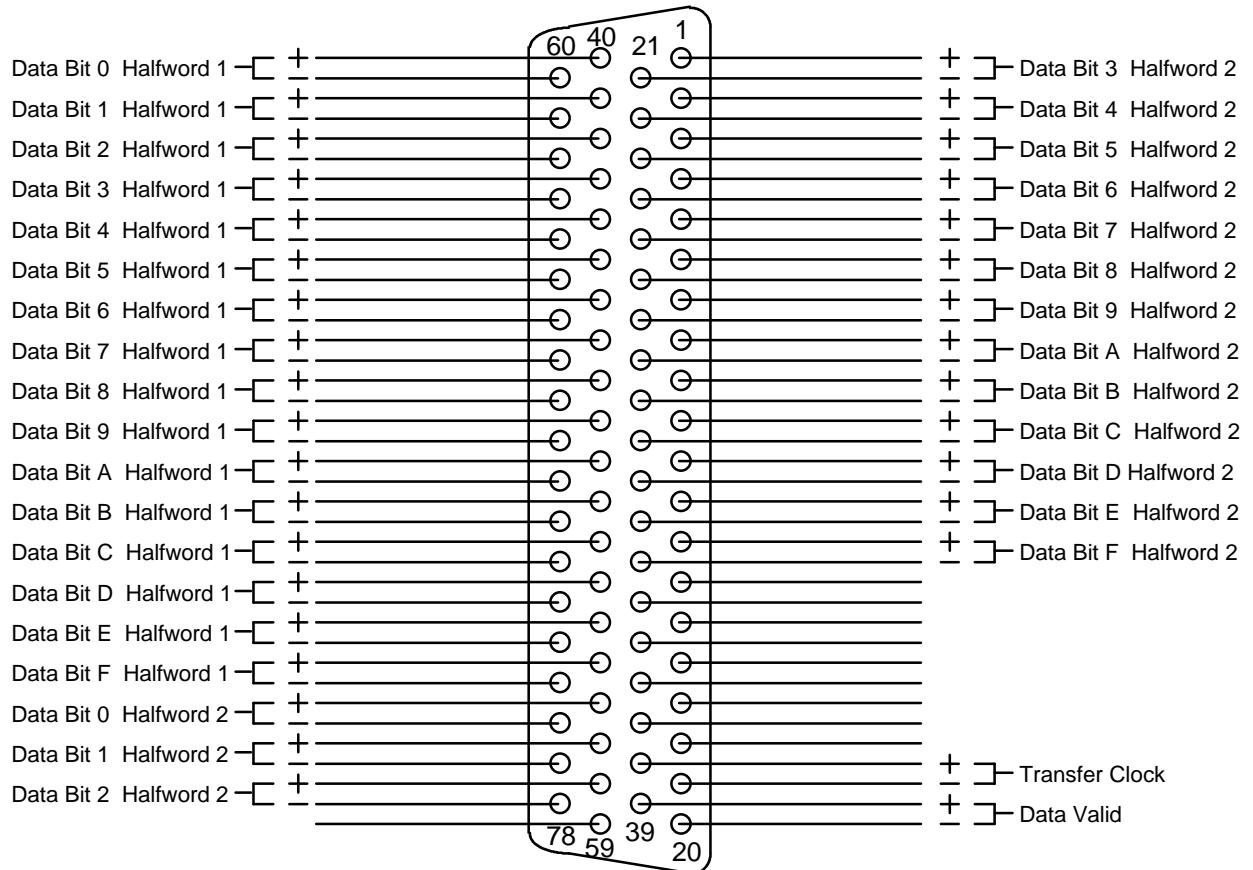


FIGURE 2.4.1

### 2.4.2 AC to WARP Signal Mapping

<u>Instrument Pin Name</u>	<u>WARP Pin Name</u>	<u>Pin Number</u>
Data Bit F Halfword2_P	AC_DB31P	13
Data Bit F Halfword2_N	AC_DB31N	33
Data Bit E Halfword2_P	AC_DB30P	12
Data Bit E Halfword2_N	AC_DB30N	32
Data Bit D Halfword2_P	AC_DB29P	11
Data Bit D Halfword2_N	AC_DB29N	31
Data Bit C Halfword2_P	AC_DB28P	10
Data Bit C Halfword2_N	AC_DB28N	30
Data Bit B Halfword2_P	AC_DB27P	9
Data Bit B Halfword2_N	AC_DB27N	29
Data Bit A Halfword2_P	AC_DB26P	8
Data Bit A Halfword2_N	AC_DB26N	28
Data Bit 9 Halfword2_P	AC_DB25P	7
Data Bit 9 Halfword2_N	AC_DB25N	27
Data Bit 8 Halfword2_P	AC_DB24P	6
Data Bit 8 Halfword2_N	AC_DB24N	26
Data Bit 7 Halfword2_P	AC_DB23P	5
Data Bit 7 Halfword2_N	AC_DB23N	25
Data Bit 6 Halfword2_P	AC_DB22P	4
Data Bit 6 Halfword2_N	AC_DB22N	24
Data Bit 5 Halfword2_P	AC_DB21P	3
Data Bit 5 Halfword2_N	AC_DB21N	23
Data Bit 4 Halfword2_P	AC_DB20P	2
Data Bit 4 Halfword2_N	AC_DB20N	22
Data Bit 3 Halfword2_P	AC_DB19P	1
Data Bit 3 Halfword2_N	AC_DB19N	21
Data Bit 2 Halfword2_P	AC_DB18P	58
Data Bit 2 Halfword2_N	AC_DB18N	78
Data Bit 1 Halfword2_P	AC_DB17P	57
Data Bit 1 Halfword2_N	AC_DB17N	77
Data Bit 0 Halfword2_P	AC_DB16P	56
Data Bit 0 Halfword2_N	AC_DB16N	76
Data Bit F Halfword1_P	AC_DB15P	55
Data Bit F Halfword1_N	AC_DB15N	75
Data Bit E Halfword1_P	AC_DB14P	54
Data Bit E Halfword1_N	AC_DB14N	74
Data Bit D Halfword1_P	AC_DB13P	53
Data Bit D Halfword1_N	AC_DB13N	73
Data Bit C Halfword1_P	AC_DB12P	52
Data Bit C Halfword1_N	AC_DB12N	72
Data Bit B Halfword1_P	AC_DB11P	51
Data Bit B Halfword1_N	AC_DB11N	71
Data Bit A Halfword1_P	AC_DB10P	50

Data Bit A Halfword1_N	AC_DB10N	70
Data Bit 9 Halfword1_P	AC_DB9P	49
Data Bit 9 Halfword1_N	AC_DB9N	69
Data Bit 8 Halfword1_P	AC_DB8P	48
Data Bit 8 Halfword1_N	AC_DB8N	68
Data Bit 7 Halfword1_P	AC_DB7P	47
Data Bit 7 Halfword1_N	AC_DB7N	67
Data Bit 6 Halfword1_P	AC_DB6P	46
Data Bit 6 Halfword1_N	AC_DB6N	66
Data Bit 5 Halfword1_P	AC_DB5P	45
Data Bit 5 Halfword1_N	AC_DB5N	65
Data Bit 4 Halfword1_P	AC_DB4P	44
Data Bit 4 Halfword1_N	AC_DB4N	64
Data Bit 3 Halfword1_P	AC_DB3P	43
Data Bit 3 Halfword1_N	AC_DB3N	63
Data Bit 2 Halfword1_P	AC_DB2P	42
Data Bit 2 Halfword1_N	AC_DB2N	62
Data Bit 1 Halfword1_P	AC_DB1P	41
Data Bit 1 Halfword1_N	AC_DB1N	61
Data Bit 0 Halfword1_P	AC_DB0P	40
Data Bit 0 Halfword1_N	AC_DB0N	60
Transfer Clock_P	AC_CLKP	38
Transfer Clock_N	AC_CLKN	19
Data Valid_P	AC_VALIDP	39
Data Valid_N	AC_VALIDN	20

## 2.5 Bit Level Timing

### 2.5.1 Rise Time

The rise time of the AC data lines is 1 nSecond min. and TBD nSecond max.

### 2.5.2 Fall Time

The fall time of the AC data lines is 1 nSecond min. and TBD nSecond max.

### 2.5.3 Clock Frequency

The data clock has two speeds 6.0 MHz and 3.0 MHz. The data clock is only set to the 6.0 MHz rate during periods that the ALI is not on and the AC is set for a 60 Hz frame rate. The data clock is set for 3.0 MHz for all other frame rates. For the slower frame rates, e.g. 2 Hz, 7.5 Hz, and 15 Hz, the data buffers may empty giving intra-frame gaps in the data coming over the RS-422 link. During these gaps, the data ready bit will remain low.

### 2.5.4 Timing Diagrams

Figures 2.5.4.1 and 2.5.4.2 show the bit level timing for data transfers with respect to the data transfer clock and the data ready signals.

FIGURE 2.5.4.1

FIGURE 2.5.4.2

## 2.6 Signal Levels

### 2.6.1 Transmit Levels

The low level output voltage of transmitted signals is 0.5V maximum. The high level output voltage of transmitted signals is 2.5V minimum.

### 2.6.2 Receive Levels

The low level output voltage of received signals is 0.3V maximum. The high level output voltage of received signals it 3.8V minimum.

## 2.7 Signal Grounding and Isolation

The signal grounding and isolation of the AC / WARP interface shall conform to Doc. No. AM149-0020(155).

## 2.8 Handling Procedures

### 2.8.1 ESD Precautions

The AC instrument hardware will be handled using standard ESD safeguards for space flight equipment.

## 2.9 EMI/EMC/RFI Specifications and Procedures

AC to WARP RS-422 Interface will comply with EO-1 Verification Plan and Environmental Specification SAI-SPEC-158

# 3 DATA LINK LAYER

## 3.1 Data Link Layer Function

The Data Link Layer defines the basic data units, usually called frames, which are present on the interface and ensures that they are transmitted free of errors from the source to the destination. The frames are created by adding headers and /or trailers to the data at the source which are recognized by the Data Link Layer service in the receiver. These frames can serve as sync patterns and also as the extra bits required for frame error detection and correction. The other principal function of this layer is flow control: managing the volume of data from source to destination so as to prevent overflow or underflow of the buffers on either end. Both flow control and error control require acknowledgment from receiver to source, and this acknowledgment scheme is defined at this layer.

## 3.2 Data Unit (Frame) Definition

### 3.2.1 Frame Data Area Size

A frame for the AC consists of a frame header of 512 half-words and three 256 X 256 pixel array samples of 1 half-word each (for a total of 3.153920 Mbits).

### 3.2.2 Frame Header Definition

The frame header is defined in Figure 3.3.2. It consists of 2 half-words all set to logic level 1 signifying a beginning of frame. The frame start is followed by mission timing data acquired from the spacecraft master clock for time stamping of the data collected. There is a frame counter for counting the frames during a certain 1 second interval. Finally, the temperature of each array as read from the on-chip temperature sensors is recorded. At the end of the frame header there are 500 half-words that are currently spares.

## LEISA/AC Data Header Format

Header: 512 Halfwords ( 16 bits/Halfword )

0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F

Frame Start - 32 Bits All Set To "1"  
 Two Halfwords

0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---

Days: Range 0-366  
 One Halfword

0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---

Hours: Range 0-23  
 One Halfword

0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---

Minutes: Range 0-59  
 One Halfword

0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---

Seconds: Range 0-59  
 One Halfword

0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F

Microseconds: Range 0-999,000  
 Microseconds: 4 MS Bits  
 Microseconds: 16 LS Bits

0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---

Offset Counter ( 8 Bits )  
 One Halfword

0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---

Focal Plane 1 Temperature ( Voltage )  
 One Halfword

0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---

Focal Plane 2 Temperature ( Voltage )  
 One Halfword

0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---

Focal Plane 3 Temperature ( Voltage )  
 One Halfword

0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---

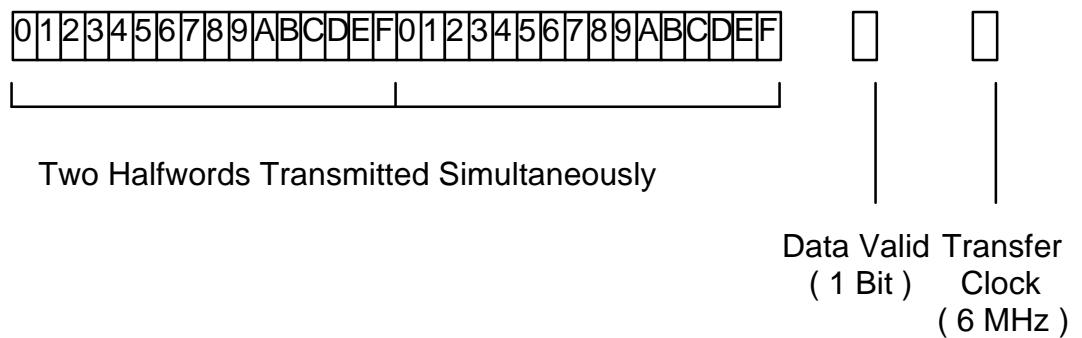
Spare: 500 Halfwords

### FIGURE 3.2.2

#### 3.2.3 Frame Trailer Definition

The LEISA/AC does not have a trailer.

#### 3.2.4 Frame Timing



### 3.3 Data Unit Timing

#### 3.3.1 Inter-Frame Gaps

The data header is constructed by the UT69R000 micro-controller at the time that the frame start command is received. The data header is transmitted across the science data bus to the WARP as soon as it is completed. Immediately following the data header, the science data is transmitted from dual port memory to the data bus. There may be inter-frame gaps in the data transmission of up to 320 usec during those times the data valid signal will remain low.

## 4 NETWORK LAYER AND APPLICATION LAYERS

TBD

**NOTE:** This section will be provided by the AC team by the April 30, 1998 timeframe and approved through a future CCR process. This section will contain sufficient information to validate data content, structure and volume from the AC interface through WARP IGSE.

Date: Fri, 23 Jan 1998 12:40:50 -0500 (Eastern Standard Time)  
From: Administrator@hst-nic.hst.nasa.gov  
Reply-to: (George Jackson/561)  
Subject: CCR:0007 - DUE: 02/13/98 ROUTINE Level-2 George Jackson/56 WWW-COMMENTS

USER : (George Jackson/561) sent the following comments on :

-----  
Date: 01/23/1998  
CCR Number: 0007  
Sponsor: D.Reuter/Code 735  
Due Date: 02/13/98

-----  
CCR Title: BASELINE EO-1 WARP AND LEISA/AC ICD-057

-----  
Remote host: 198.118.115.46 Email Address:

-----  
APPROVAL STATUS: APPROVED WITH COMMENTS  
Note: Hard Copy Marked Up Graphics Mailed Separately

-----  
COMMENTS: Make following changes: (Separate hard copies also submitted).

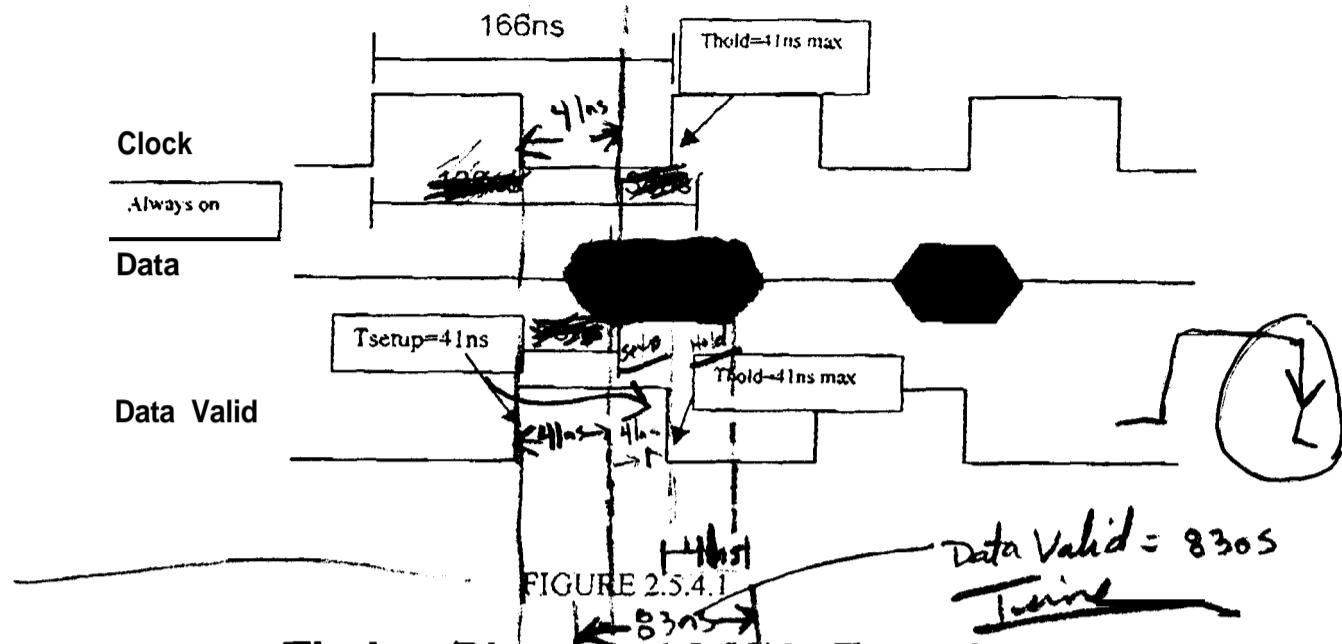
Section 2.5.4 Timing Diagrams: Add at the end of section:  
"The Data Valid bit is a gated clock which is only active when data is on the bus. The Data Valid bit will transition from a logic high to logic low to induce a valid data transfer, otherwise it will remain at a logic low."

#### Section 4 Network Layer and Application Layers

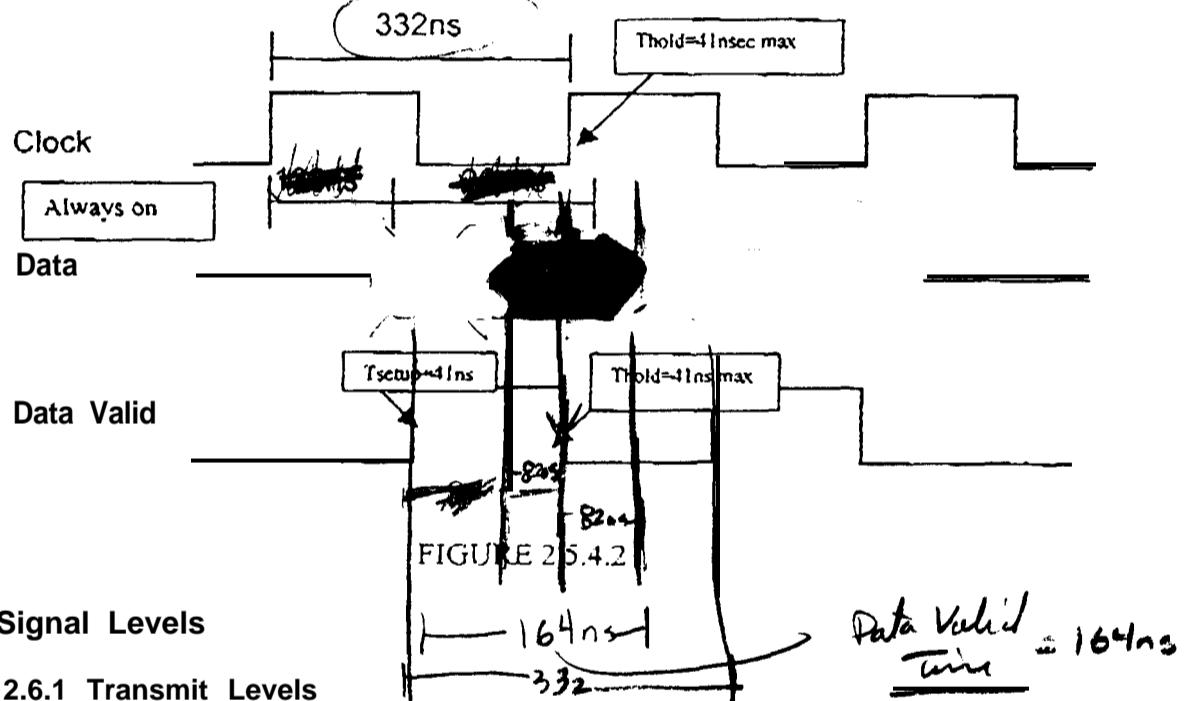
Change from: NOTE: This section will be provided by the AC team by the April 30th, 1998 time frame and approved through a future CCR process.

To: NOTE: This section will be provided by the AC team by April 30th, 1998 and approved through a future CCR process.

## Timing Diagram ( 6 MHz Transfer )



## Timing Diagram ( 3 MHz Transfer )



### 2.6 Signal Levels

#### 2.6.1 Transmit Levels

The low level output voltage of transmitted signals is 0.5V maximum. The high level output voltage of transmitted signals is 2.5V minimum.

4

#### 2.6.2 Receive Levels

The low level output voltage of received signals is 0.3V maximum. The high level output voltage of received signals is 3.8V minimum.

01/21/98

Date: Thu, 05 Feb 1998 18:23:19 -0500 (Eastern Standard Time)  
From: Administrator@hst-nic.hst.nasa.gov  
Reply-to: (Dennis Reuter/ Code 693)  
Subject: CCR:0007 - DUE: 02/13/98 ROUTINE Level-2 Dennis Reuter/ Code 69 WWW-COMMENTS

USER : (Dennis Reuter/ Code 693) sent the following comments on :

-----  
Date: 02/05/1998  
CCR Number: 0007  
Sponsor: T. Smith/Code 735  
Due Date: 02/13/98

-----

CCR Title: BASELINE EO-1 WARP AND LEISA/AC ICD-057

-----

Remote host: 128.183.124.13 Email Address: dennis.reuter@gsfc.nasa.gov

-----

APPROVAL STATUS: APPROVED WITH COMMENTS

Note:

-----

COMMENTS: 1) I would prefer to move section 4, which is a TBD section dealing with the order of the data coming from the AC, to the spacecraft to ground ICD. The information which would be contained in this section does not affect the WARP interface in any way, and is most useful in the level 0 processing.

2) Very minor: in sections 2.5.3 and 2.5.4 the data valid signal is referred to as data ready. Data ready should be changed to data valid here and anywhere else it may occur.

EO-1 CCR SPONSOR RECOMMENDATION FORM

CCR NUMBER: 0007

CCR TITLE: B/L EO-1 WARP & LEISA ICD-057

CCR SPONSOR: D. Reuter/GSFC

SPONSOR RECOMMENDATION: (Make changes to document where indicated, reference Sponsor Comments for changes to be implemented.)

Approve \_\_\_\_\_ Approve with Change  X Disapprove \_\_\_\_\_

SPONSOR/ORGANIZATION: D. Reuter/693

DATE: 3/3/98

COMMENTS RECEIVED:

**George Jackson/561:** Make the following changes:

Sent 2.5.4 Timing Diagrams: Add at the end of the section:

"The Data Valid bit is a gated clock which is only active when data is on the bus. The Data Valid bit will transition from a logic high to logic low to induce a valid data transfer, otherwise it will remain at a logic low."

Sponsor Response: **Agree.** Incorporate as specified.

Section 4 Network Layer and Application Layers:

Change From: NOTE: This section will be provided by the AC team by the April 30<sup>th</sup>, 1998 time frame and approved through a future CCR process.

To: NOTE: This section will be provided by the AC team by April 30, 1998 and approved through a future CCR process.

Sponsor Response: **Agree.** See Sponsor recommendation to delete section entirely.

**Steve Graham/Code 718:** Add: The following Timing Diagram to Figure 2.5.4.2 (See attachment)

Sponsor Response: **Agree.** Add section as specified.

Sponsor comments:

Incorporate the above suggested changes as written.

Sponsor's incorporated changes: Delete Section 4, which is a TBD section dealing with the order of the data coming from the AC, the spacecraft to ground ICD. The information which would be contained in this section does not affect the WARP interface in any way, and is most useful in the level 0 processing.

Very minor: ins sections 2.5.3 and 2.5.4 the data valid signal is referred to as data ready. Data ready should be changed to data valid here and anywhere else it may occur.

